

## **ABSTRACT OF THE DISCLOSURE**

In a preferred embodiment, the invention provides a circuit and method for improving the soft error rate in a dual-port read SRAM cell. A write-only transfer device is connected to a cross-coupled latch, a first wordline, and a first bitline. A  
5 first read-only transfer device is connected to a second bitline, a second wordline, and a first pull-down device. A second read-only transfer device is connected to the first bitline, the first wordline, and a second pull-down device. A clear memory transfer device is connected to the cross-coupled latch, a third bitline, and a third pull-down device. This configuration allows a reduction in the size of a dual-port SRAM cell  
10 with little or no reduction in the read access time of the cell. The reduction in size also reduces SER by reducing the cross-sectional, p/n junction area exposed to radiation.